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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/554,106	08/28/2006	Hiroya Kobayashi	046124-5433	6587

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EXAMINER	
AGGARWAL, YOGESH K	

ART UNIT	PAPER NUMBER
2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/554,106	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	YOGESH K. AGGARWAL	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/24/2008,09/28/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamada et al. (US Patent # 6,768,516).

[Claim 1]

Yamada teaches a solid-state imaging apparatus comprising (figure 2) a solid-state imaging element (image sensor 4), having an energy ray sensitive portion; a signal processing circuits (9), processing signals output from said solid-state imaging element; and a package (21), housing the solid-state imaging element (4) and the signal processing circuit (9), wherein the signal processing circuit is positioned at a planar portion of the package that differ from a planar portion at which the solid-state imaging element is positioned (figure 2, col. 3line 60-col. 4 line 50).

[Claim 2]

Yamada teaches a solid-state imaging apparatus (figure 2) comprising: a solid-state imaging element (4), having an energy ray sensitive portion; a signal processing circuit (9), processing signals output from the solid-state imaging element; and a package (21), housing the solid-state imaging element and the signal processing circuit, wherein the package has a first planar portion and a second planar portion, formed to be stepped with respect to the first planar portion, and

wherein the solid-state imaging element is positioned at the first planar portion, and the signal processing circuit is positioned at the second planar portion (See figure 2, col. 3line 60-col. 4 line 50).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US Patent # 6,768,516) in view of Throngnumchai et al. (US Patent # 5,705,807).

[Claims 3 and 4]

Yamada fails to teach wherein the signal processing circuit includes a load resistor that is electrically connected to an output terminal of the solid-state imaging element and the other end of which is grounded; and a buffer amplifier, having a bipolar transistor that is electrically connected to the output terminal of the solid-state imaging element. However Throngnumchai teaches in figure 45 a photodiode 31 that has a load resistor 31 that is electrically connected to an output terminal of the solid-state imaging element 31 and the other end of which is grounded; and a buffer amplifier (32), having a bipolar transistor (M1 or M2) that is electrically connected to the output terminal of the solid-state imaging element 31 (col. 29 lines 19-48, figure 45). Therefore taking the combined teachings of Yamada and Throngnumchai, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have used a load resistor that is electrically connected to an output terminal of the solid-state imaging element and

the other end of which is grounded; and a buffer amplifier, having a bipolar transistor that is electrically connected to the output terminal of the solid-state imaging element in order to reduce the cost of a system since it is easy to integrate the circuit without the need for any bulky capacitors.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOGESH K. AGGARWAL whose telephone number is (571)272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571)-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Yogesh K Aggarwal/
Primary Examiner, Art Unit 2622